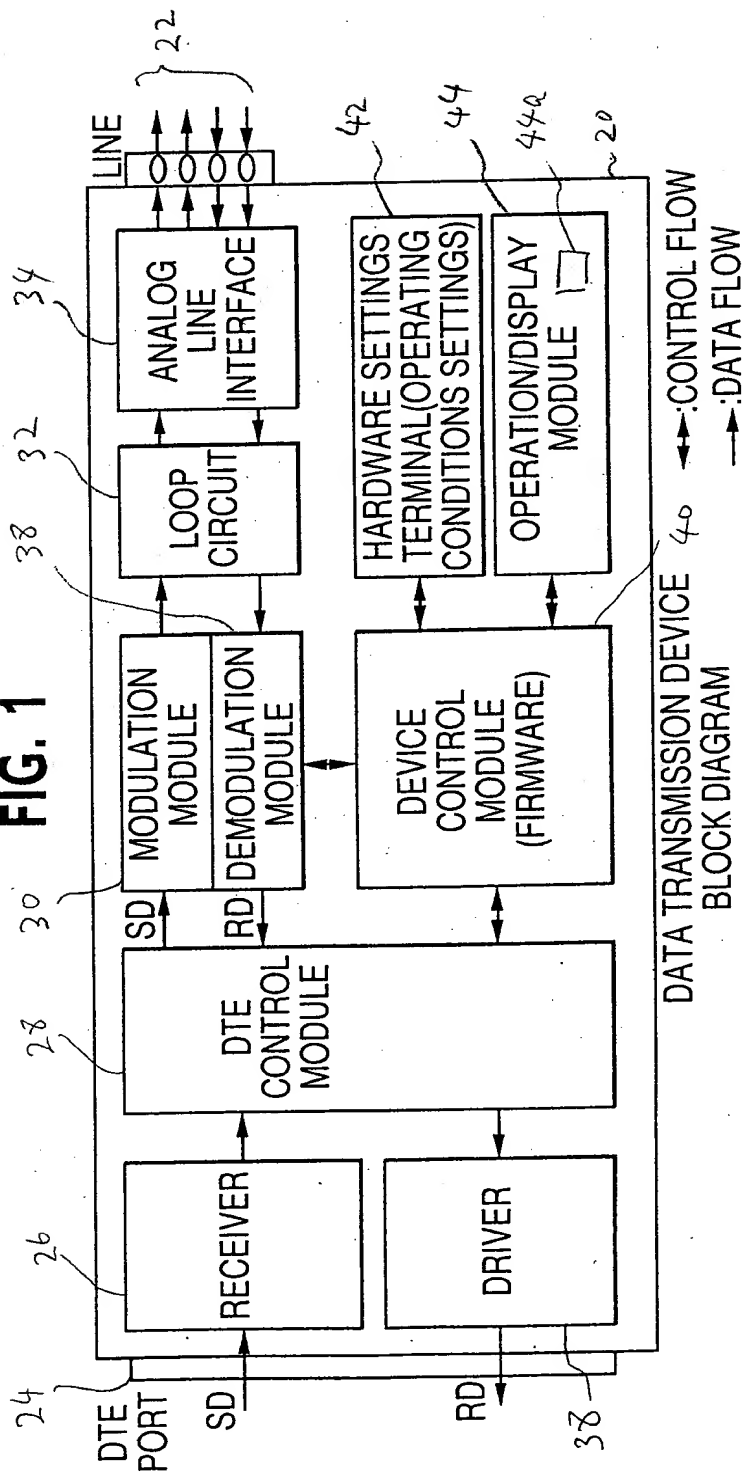
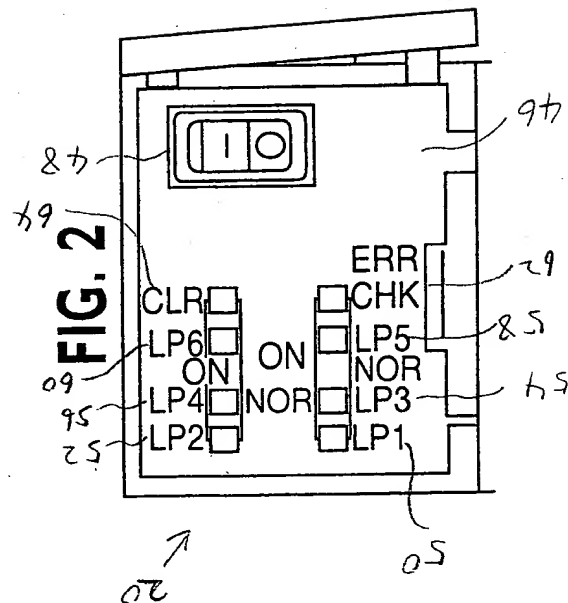


**FIG. 1**



**FIG. 2**



# LIST OF SETTING SWITCHES

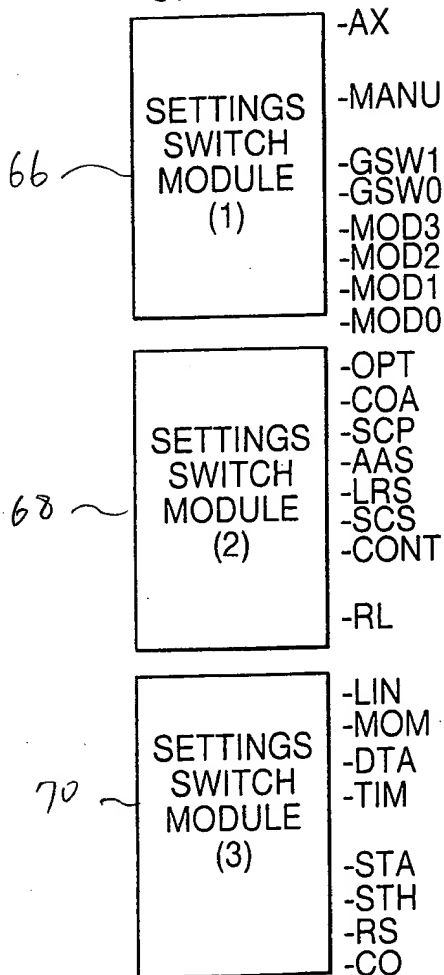
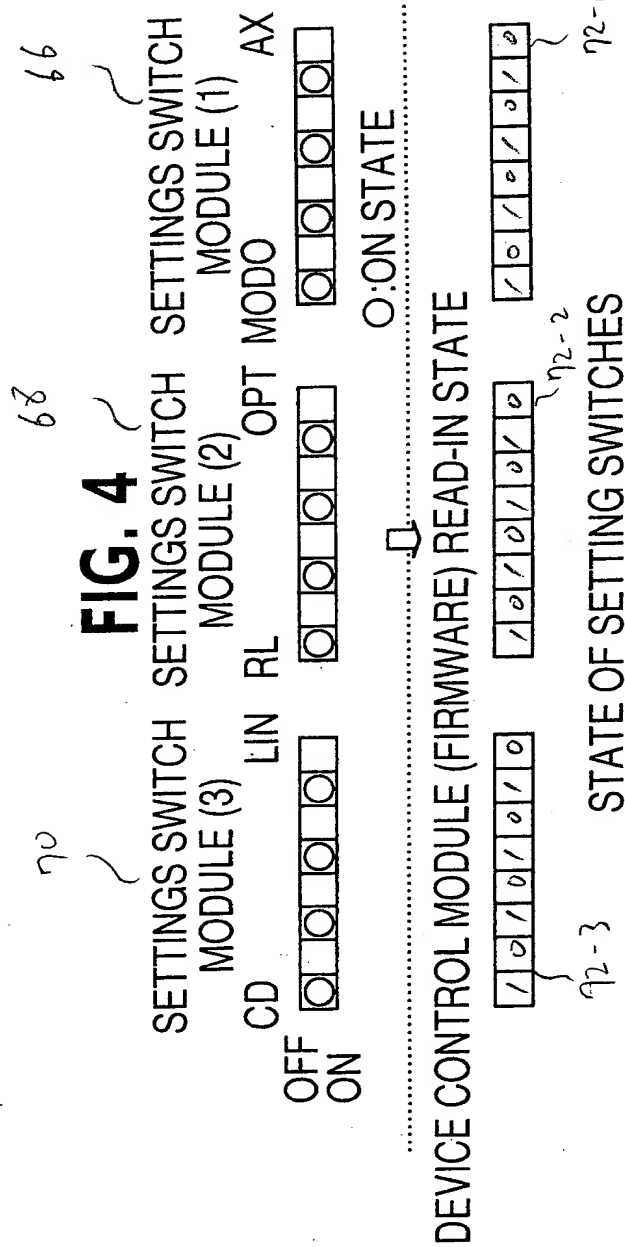


FIG. 3

- :73AX2A MODE/73AX2 MODE/73AX MODE SWITCH (COMBINED WITH CORE BOARD SETTINGS)
- :SETTING FOR CHECK OF RECEIVED LEVEL MANUAL ADJUSTMENTS
- : } RECEIVED LEVEL RANGE SETTINGS
- : } DTE-SIDE TRANSMISSION SPEED SETTINGS
- :DTE INTERFACE SETTINGS
- :NOT IN USE
- :NOT IN USE
- :NOT IN USE
- :NOT IN USE
- :CS DELAY TIME IN RELATION TO RS
- :SETTINGS TO CHECK FOR CONTINUOUS TESTING DURING COUNTER RETURN TEST
- :SETTINGS TO CHECK FOR COUNTER RETURN TEST FUNCTION
- : } DATA TRANSMISSION CLOCK SOURCE SETTINGS
- :ORIGINATION STATION MODEM SEND SIGNAL TIMING SETTINGS
- :STI/TANDEM OPERATION SETTINGS
- :NOT IN USE
- :NOT IN USE
- :CARRIER DETECTION



72

Fig. 5A

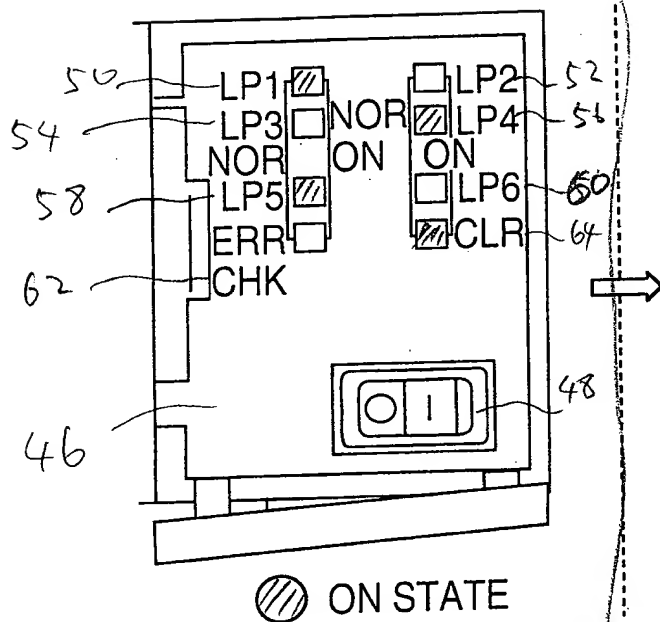
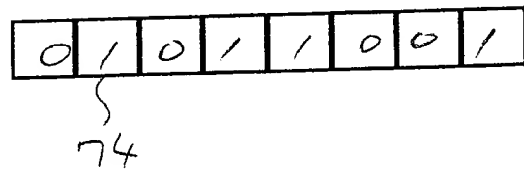


Fig. 5B

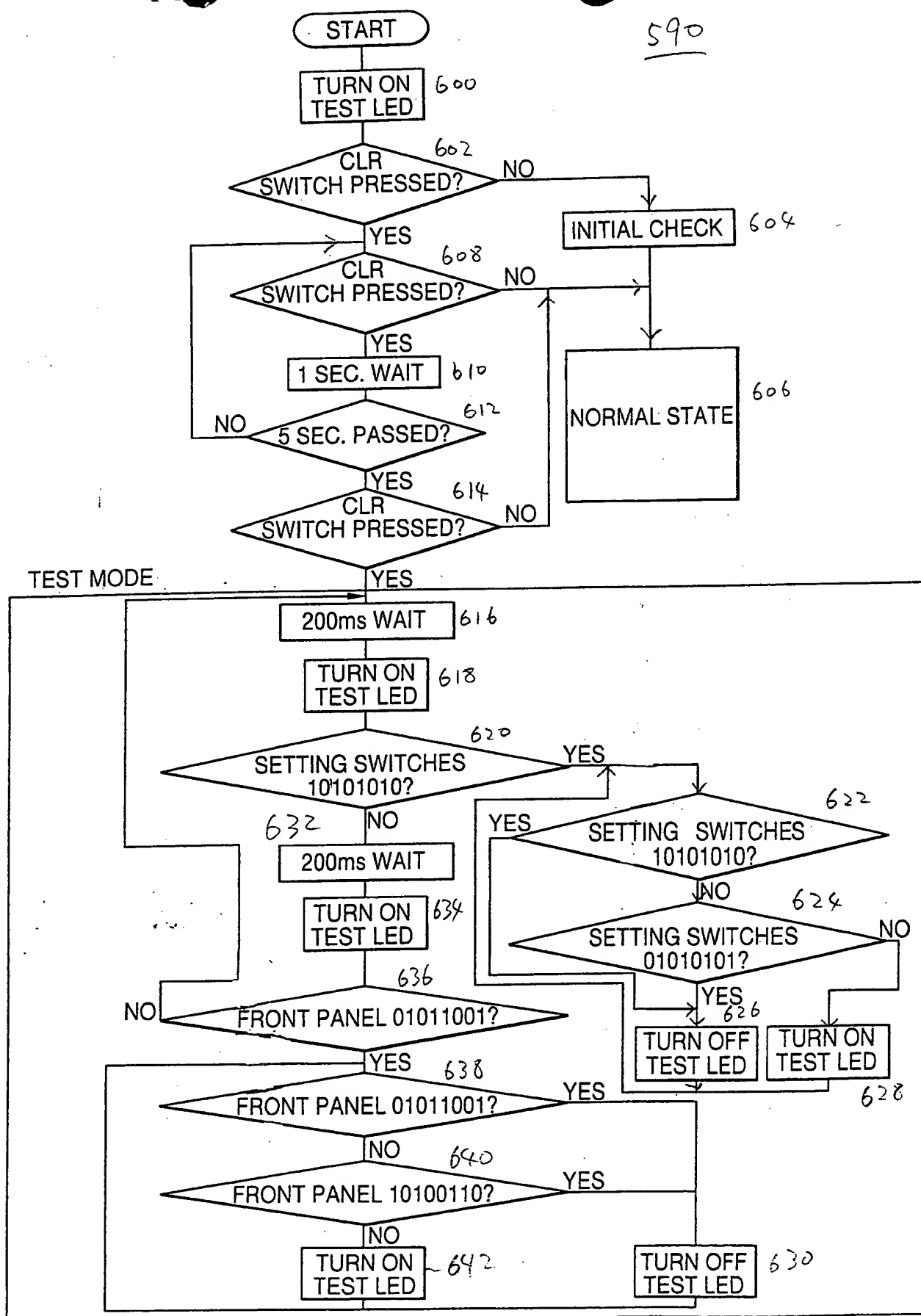
DEVICE CONTROL MODULE (FIRMWARE)  
READ-IN STATE



STATE OF FRONT PANEL SWITCHES

# FIG. 6

590



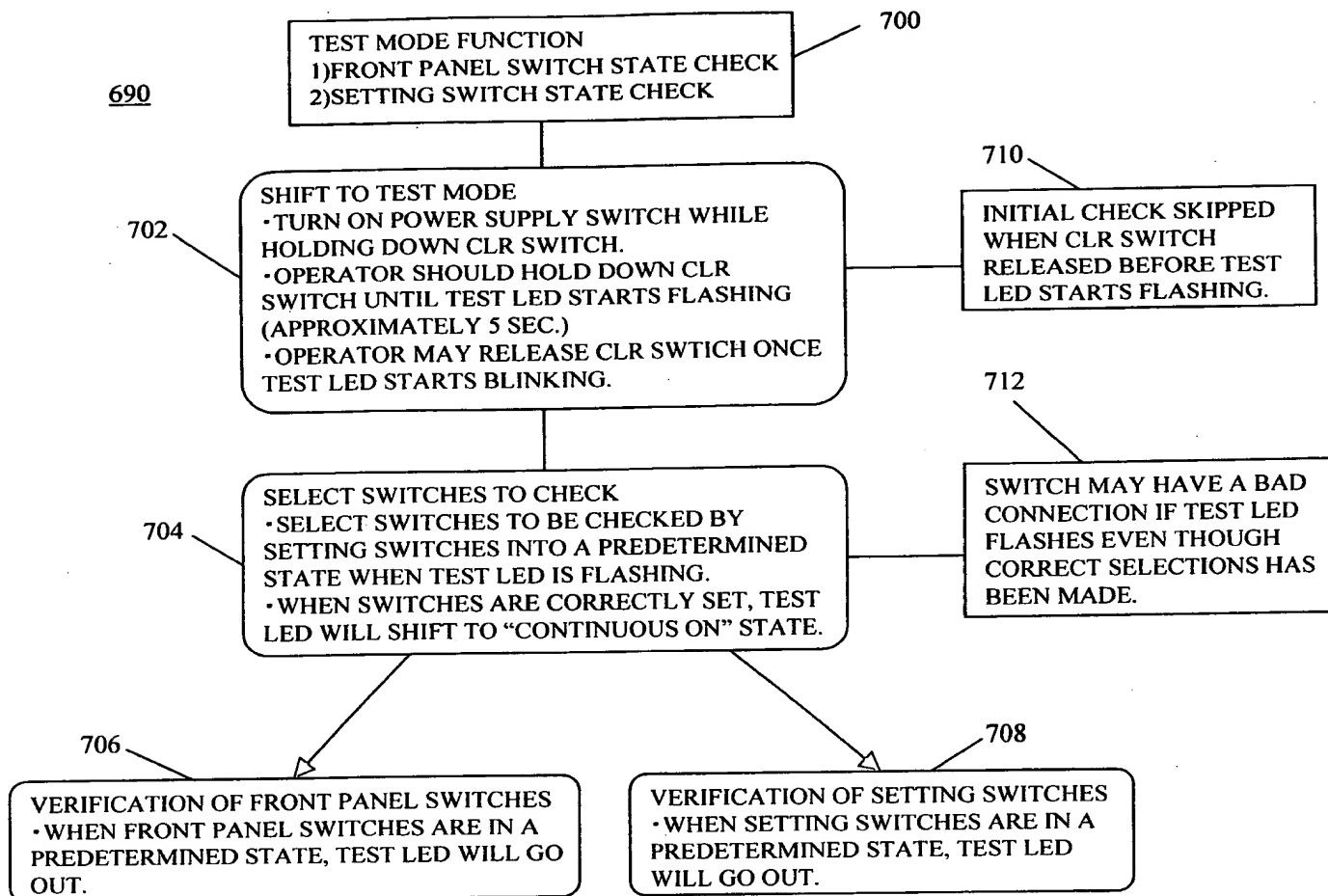


Fig.7A

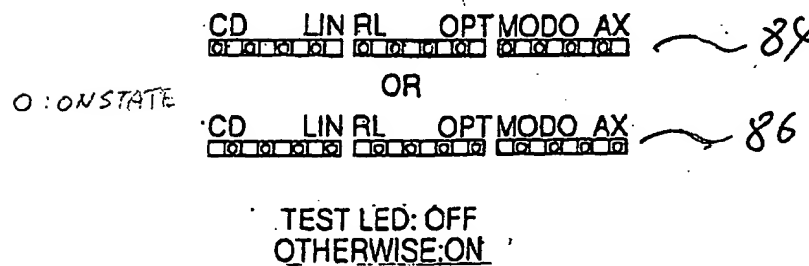
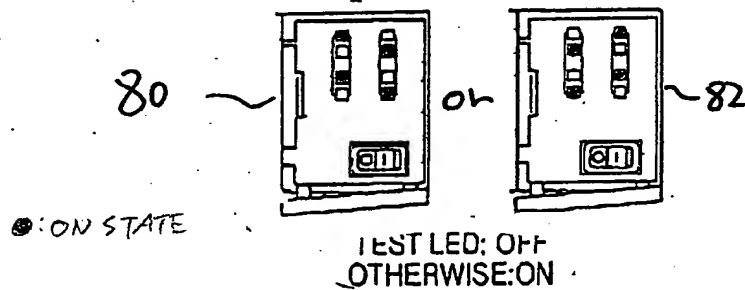
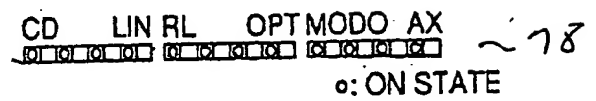
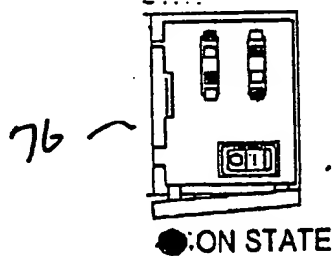


Fig 7B

09752527 0440  
T0770 425260

**FIG. 8**

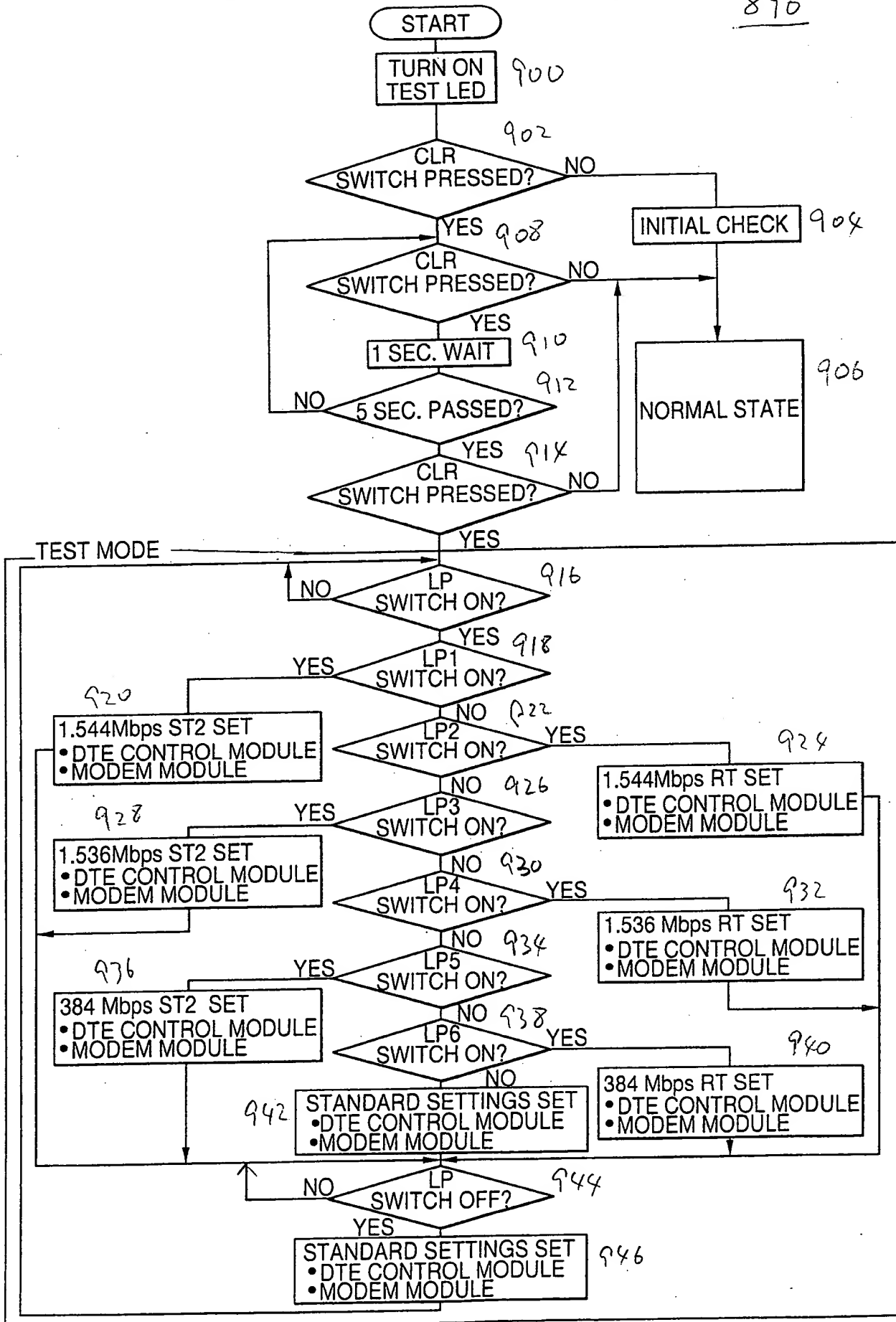
800

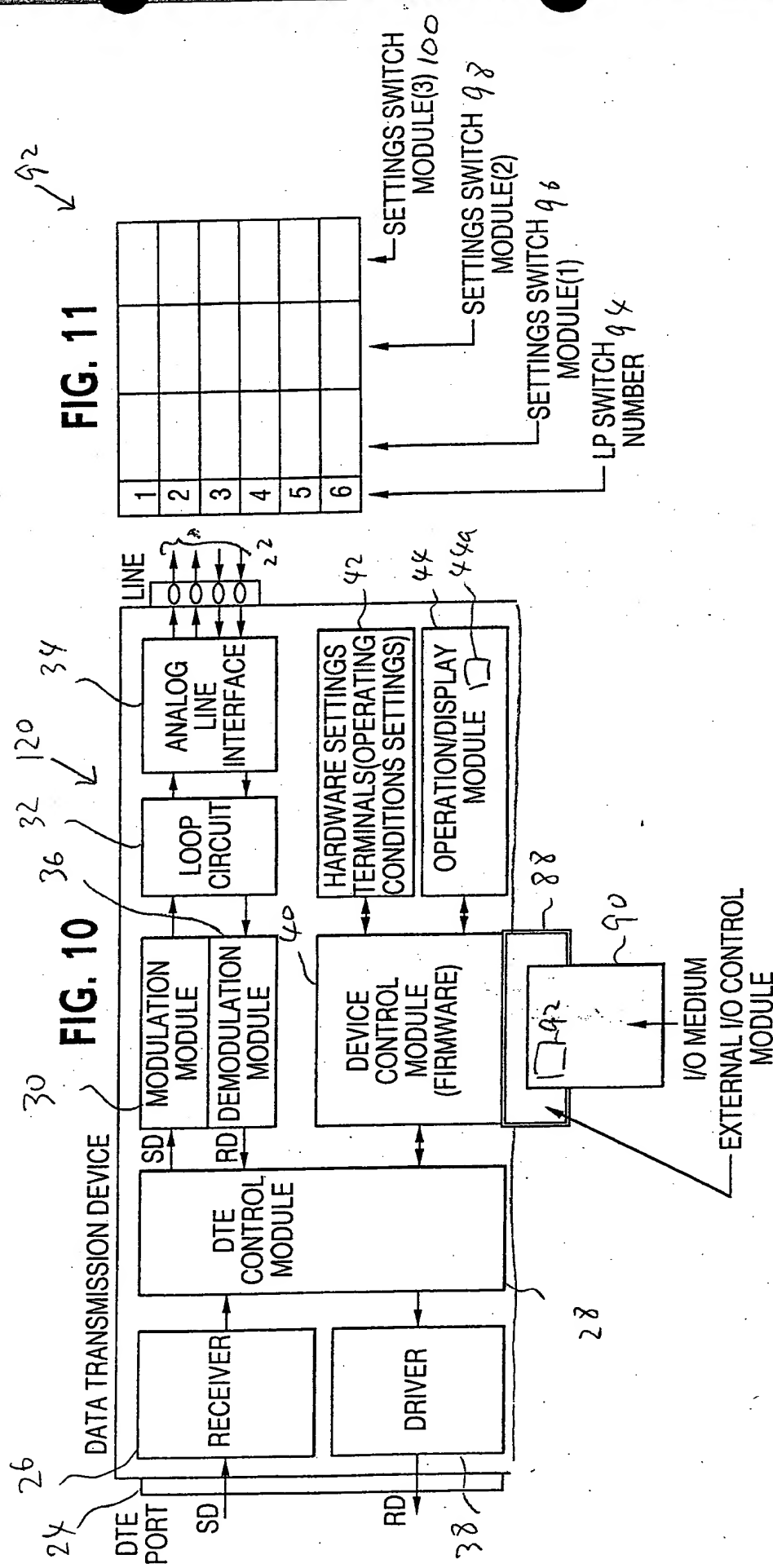
ORIGINATION STATION		DESTINATION STATION	
SWITCH	OPERATING CONDITIONS	OPERATING CONDITIONS	SWITCH
LP1	1.544 Mbps ST2	1.544 Mbps RT	LP2
LP3	1.536 Mbps ST2	1.536 Mbps RT	LP4
LP5	384 kbps ST2	384 kbps RT	LP6



FIG. 9

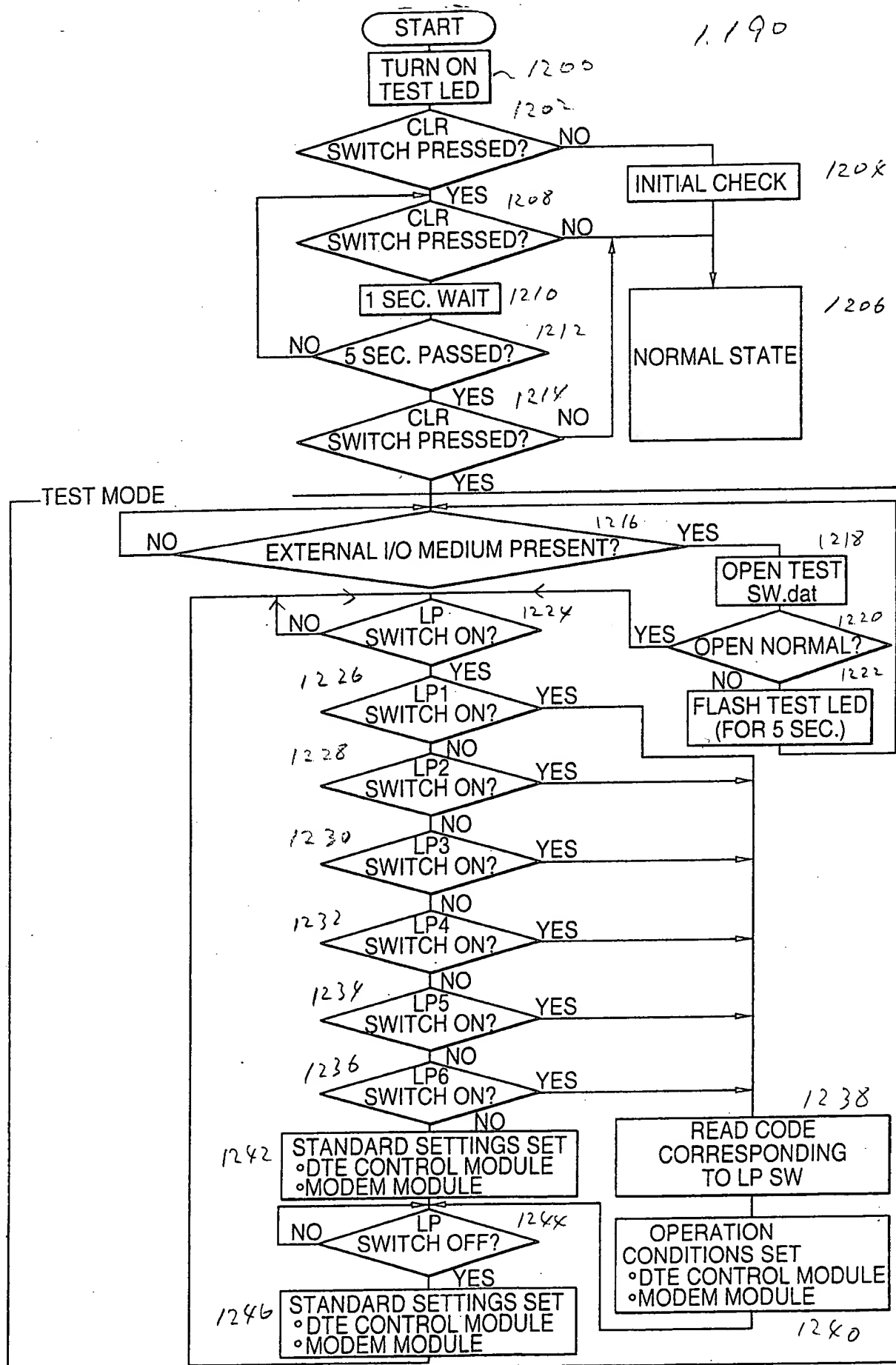
890





↔: CONTROL FLOW  
 →: DATA FLOW

FIG. 12



FIG

13A

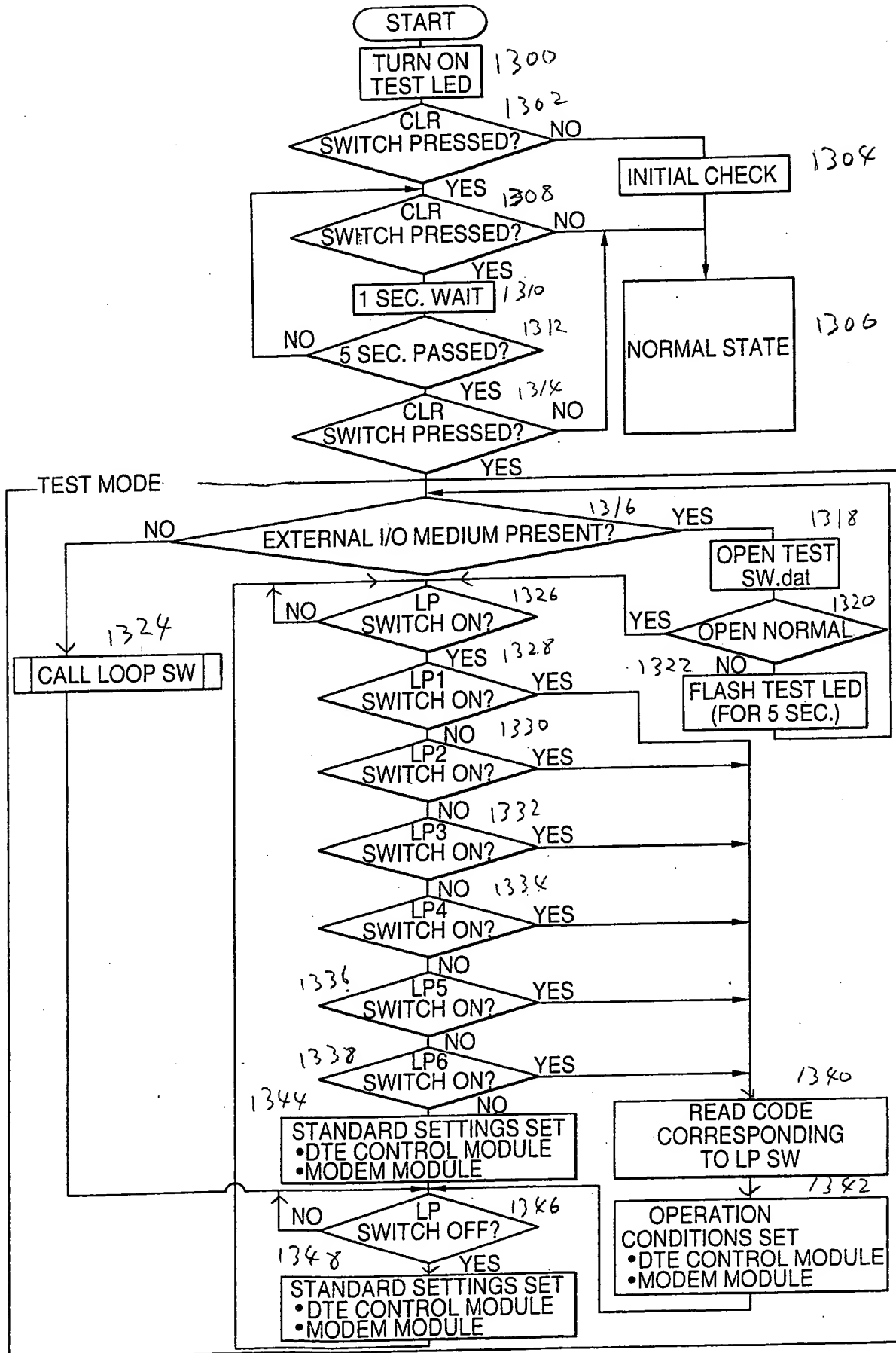


FIG. 13B

132x

